## 7853USF.RTF

10

## WHAT IS CLAIMED IS:

- 1. A non-volatile memory, comprising:
- a substrate;
- a word-line on the substrate;
- 5 a charge trapping layer between the substrate and the word-line;
  - a contact disposed over the substrate electrically connecting with the word-line; and
  - a protective metal line electrically connecting with the contact and with a grounding doped region in the substrate, wherein the protective metal line has a first resistance higher than a second resistance of the word-line.
  - 2. The non-volatile memory of claim 1, wherein the protective metal line has a first width smaller than a second width of the word-line.
  - 3. The non-volatile memory of claim 1, wherein the protective metal line has a first thickness smaller than a second thickness of the word-line.
- 4. The non-volatile memory of claim 1, wherein the protective metal line is electrically connected with the grounding doped region via another contact.
  - 5. The non-volatile memory of claim 1, wherein the charge trapping layer comprises a silicon oxide/silicon nitride/silicon oxide (ONO) composite layer.
    - 6. The non-volatile memory of claim 1, wherein the word-line comprises:
- a polysilicon line on the charge trapping layer; and a metal silicide line on the polysilicon line.
  - 7. The non-volatile memory of claim 6, wherein the metal silicide line comprises tungsten silicide (WSi<sub>x</sub>).
    - 8. A method for fabricating a non-volatile memory, comprising the steps of:

## 7853USF.RTF

10

forming a non-volatile memory cell on a substrate;

forming a grounding doped region in the substrate;

forming a first contact on the substrate electrically connecting with the grounding doped region;

forming a second contact on the substrate electrically connecting with a wordline of the non-volatile memory cell;

forming a protective metal line having a first resistance higher than a second resistance of the word-line over the substrate, wherein the protective metal line is electrically connected with the grounding doped region via the first contact and is electrically connected with the word-line via the second contact; and

applying a large current to blow the protective metal line.

- 9. The method of claim 8, wherein forming the protective metal line comprises: forming a metal layer over the substrate; and patterning the metal layer to form the protective metal line.
- 10. The method of claim 8, wherein forming the non-volatile memory cell comprises:

forming a charge trapping layer on the substrate;

forming a polysilicon layer on the charge trapping layer;

forming a metal silicide layer on the polysilicon layer; and

- patterning the metal silicide layer, the polysilicon layer and the charge trapping layer to form the word-line.
  - 11. The method of claim 10, wherein the charge trapping layer comprises a silicon oxide/silicon nitride/silicon oxide (ONO) composite layer.
    - 12. The method of claim 10, wherein the metal silicide layer comprises tungsten

## 7853USF.RTF

silicide (WSi<sub>x</sub>).

- 13. The method of claim 8, further comprising forming a dielectric layer over the substrate after the grounding doped region is formed in the substrate.
- 14. The method of claim 13, wherein the dielectric layer comprises borophosphosilicate glass.